UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/551,266	09/29/2005	Toshiro Akino	9694D-000025/US	3385

30593 7590 10/14/2008

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 8910
RESTON, VA 20195

EXAMINER	
O TOOLE, COLLEEN J	

ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
10/14/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/551,266	AKINO, TOSHIRO	
	Examiner	Art Unit	
	COLLEEN O'TOOLE	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☒ Claim(s) *1* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 1, 2008 has been entered.

Claim Objections

2. Claim 1 is objected to because of the following informalities: In line 22, "correct" should be replaced with --current--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jin et al. ("On The Power Dissipation in Dynamic Threshold Silicon-on-Insulator CMOS Inverter," IEEE Transactions on Electron Devices, Vol. 45, No. 8, August 1998, hereafter Jin) in view of Ishibashi et al. (U.S. Patent 6,864,539, hereafter Ishibashi), and further in view

of Shimomura et al. (JP10-189957 as listed in the Information Disclosure Statement filed September 29, 2005).

Claim 1: Jin teaches a lateral bipolar CMOS integrated circuit comprising:

an inverter circuit (Figure 3) comprising an n-channel MOS transistor (transistor in stage n-1 connected to GND) and a p-channel MOS transistor (transistor in stage n-1 connected to Vdd), and having four terminals of:

a gate input terminal Vin ("1" connected to stage n-1) connected with the gates of the n-channel MOS transistor and the p-channel MOS transistor;

an output terminal Vout ("0" connected between stages n-1 and n) connected with the drains of the n-channel MOS transistor and the p-channel MOS transistor;

a p-type base terminal connected with a p-type substrate of the n-channel MOS transistor (node between two diodes connected to the source and drain of the transistor in stage n-1 connected to Vdd); and

an n-type base terminal connected with an n-type substrate of the p-channel MOS transistor (node between two diodes connected to the source and drain of the transistor in stage n-1 connected to GND),

wherein the n-channel MOS transistor operates in a hybrid mode which is the hybrid of an operation mode of the MOS transistor and an operation mode of an npn lateral bipolar transistor which is inherent in the n-channel MOS transistor, and

the p-channel MOS transistor operates in a hybrid mode which is the hybrid of an operation mode of the MOS transistor and an operation mode of a pnp lateral bipolar transistor which is inherent in the p-channel MOS transistor. The inverter chain in

Figure 3 teaches the structure of n-channel and p-channel MOS transistors and will inherently function in a hybrid mode.

Jin does not teach a first or second current source. Ishibashi teaches an inverter circuit (Figure 6), comprising:

a current source (4, Ibn) connected with the p-type base terminal (Vbn, p-well 20) of the n-channel MOS transistor (2); and

a current source (3, Ibp) connected with the n-type base terminal (Vbp, n-well 10) of the p-channel MOS transistor (1). Ishibashi further teaches in the details of Figure 6 shown in Figure 7, that the current sources 3 and 4 can be individually controlled by control signals Cbn and Cbp (column 10 lines 66-67, column 11 lines 1-5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the current sources taught by Ishibashi in the inverter circuit taught by Jin to increase the speed of the circuit (column 1 lines 19-22).

Ishibashi does not specifically teach that the current sources are maintained at about 0 when the input voltage to the gate input terminal is approximately constant at a high level and constant at a low level. Shimomura teaches an inverter and body biasing control circuits 103 and 104 (Figure 2). Shimomura further teaches biasing the body of transistors 101 and 102 only during transitions of the input and output of the inverter ([0016]). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the body biasing control signals taught by Shimomura in the combined circuit taught by Jin and Ishibashi to minimize the power dissipation of the current source circuit ([0016]).

Claim 2: Jin further teaches that the gate input terminal ("1" connected to stage n-1), the p-type base terminal and the n-type base terminal are input terminals of the inverter circuit (Figure 3), and the output terminal ("0" connected between stages n-1 and n) is an output terminal Vout is an output terminal of the inverter circuit (Figure 3), and

the inverter circuit outputs, at the output terminal ("0" connected between stages n-1 and n), a high-level or low-level voltage fed to the gate input terminal as an inverted level voltage (Figure 3).

Claim 3: The combined circuit further teaches that when the input voltage to the gate terminal switches from low level to the high level, a forward pulse current flows from the current source connected with the p-type base terminal of the n-channel MOS transistor to the p-type base terminal in synchronization to switching (column 9 lines 51-67, column 10 lines 1-8 of Ishibashi, [0016] of Shimomura) and

When the input voltage to the gate input terminal switches from the high level to the low level, a forward pulse current flows from the current source connected with the n-type base terminal of the p-channel MOS transistor to the n-type base terminal in synchronization to switching (column 10 lines 9-29 of Ishibashi, [0016] of Shimomura).

Claim 4: Jin further teaches a voltage source (Vdd, Figure 3) and a ground source (GND, Figure 3). Jin does not teach two current sources. Ishibashi teaches a current source (4; Figure 7) connected with the p-type base terminal (Vbn) of the n-channel

MOS transistor (2) is formed by a pull-up n-channel MOS transistor (40) comprising a source terminal, a drain terminal and a substrate terminal, the drain terminal is connected with the p-type base terminal (Vbn), and the source terminal and the substrate terminal are connected with the voltage source (Vdd), and the current source (3) connected with the n-type base terminal (Vbp) of the p-channel MOS transistor (1) is formed by a pull-down n-channel MOS transistor (34) comprising a source terminal, a drain terminal and a substrate terminal, the drain terminal is connected with the n-type base terminal (Vbp), and the source terminal and the substrate terminal are connected with the ground source (Vss).

Claim 5-8: Shimomura further teaches that the inverter circuit comprising the n-channel MOS transistor and the p-channel MOS transistor is used as a CMOS standard cell in the operation mode of the MOS transistor, but is used in the hybrid mode when a large load is connected with an output from the CMOS standard cell ([0015, 0016]). It is noted that claims 5 through 8 recite the same limitation and only differ in their parent claims.

Response to Arguments

5. Applicant's arguments, filed August 1, 2008, with respect to the rejection(s) of claims 1-4 under Jin in view of Yamaguchi have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Jin in view of Ishibashi.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to COLLEEN O'TOOLE whose telephone number is (571)270-1273. The examiner can normally be reached on M-F 8:30-5:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on (571) 272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/QUAN TRA/
Primary Examiner, Art Unit 2816

/C. O./
Examiner, Art Unit 2816